NES controller-port bridge, v2b

The two-port bridge. It is v1b plus a second port with its own register, a second output register on the same SPI chain, and an LM1881 sync separator whose 5 V outputs go straight into the UNO, so a poll can be placed against a field and a line rather than only against a latch index. Everything is still on one 5 V rail and there is not one level shifter on any sheet.

This is a drawing, not a build. Nothing here has been made; v1b is the one on the bench. What this package is for is ordering the parts, cutting the board, and having something to build from when v1b's fourteen steps are done.

Nothing is placed or typed by hand. The schematic's arrangement is authored and its coordinates come from the parts' own measured sizes; the wiring list and the parts list are read back out of that same file. A sheet that would print its smallest text below 5 pt is refused rather than shrunk, which is why this schematic is on four sheets: eleven parts and 42 nets do not fit on one page anybody can print.

Sheets

SHEET	TITLE	PAPER	HOW IT IS MADE
1	Cover and sheet index	letter	this sheet
2	Bridge v2b, sheet 1: port 1	letter	schematic
3	Bridge v2b, sheet 2: port 2	letter	schematic
4	Bridge v2b, sheet 3: the UNO and the registers	letter	schematic
5	Bridge v2b, sheet 4: sync, the pads and the trigger	letter	schematic
6	Wiring list, v2b	letter	derived from the schematic
7	Wiring list, v2b (continued)	letter	derived from the schematic
8	Parts list	letter	derived from the schematic
9	One poll, as timing lanes	ANSI B	schematic

REV	DATE	REVISION
-	2026-09-08	v2 redrawn for the UNO: no 245, no C6, one rail
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-	2026-09-09	placed and poured as a board, signal traces stil...
A	2026-09-10	four letter sheets, coordinates derived not typed

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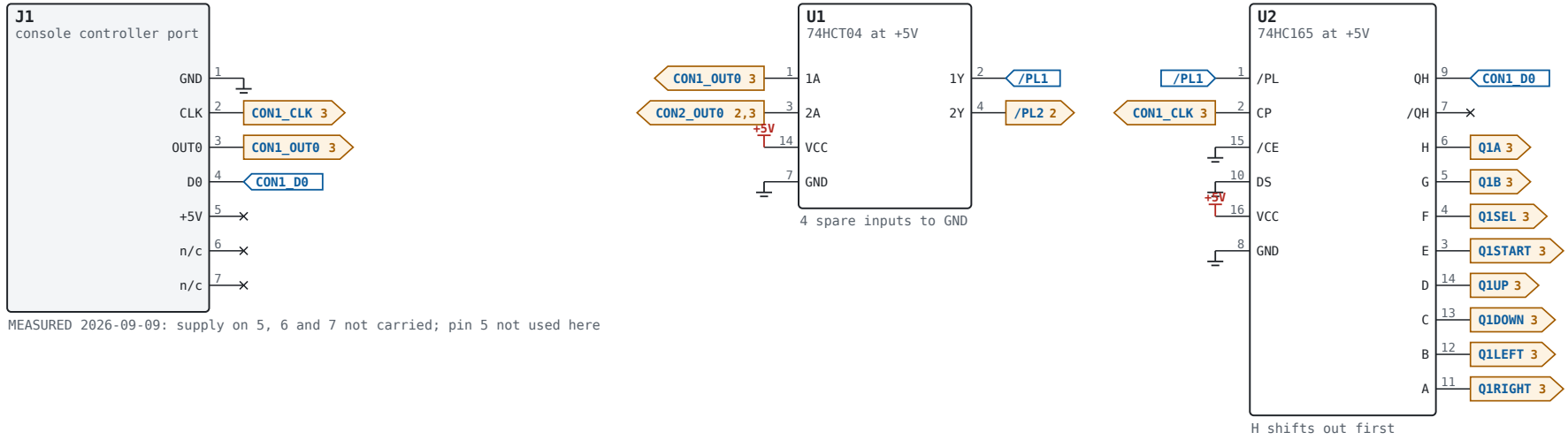
SHEET TITLE
Cover and sheet index

DRAWING NO.	REV	DATE	SHEET
TM-NESB-002	A	2026-11-04	1 of 9

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

v1b plus a second 165/595 pair on the same SPI chain and an LM1881 whose 5 V outputs go straight into the UNO. 2026-09-09. Not built.

PORT 1: THE CONSOLE PORT, THE INVERTER AND ITS REGISTER, ALL AT +5V



WHAT THE CONSOLE DOES, AND WHAT MAY NOT MOVE WHILE IT DOES IT

OUT0 high: U1 drives /PL1 low and U2 loads its eight inputs. It is transparent while low, so the byte must already be on U5's outputs (sheet 3). OUT0 falls, /PL1 goes high, the byte is held, and QH shows A. Each CLK rising edge shifts the next bit out. DS to GND means the ninth read and later return 1 to the console, which is what an original pad does. Pressed is LOW.
Port 2 is the same circuit on sheet 2. It shares this inverter, U1's second channel, and the SPI chain; it has its own register, its own pad and its own D0.

bench-v2b-1.svg ansi-a placed at 75% drawn by tools/draw-schematics.py

REV	DATE	REVISION
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-	2026-09-09	placed and poured as a board, signal traces stil...
A	2026-09-10	four letter sheets, coordinates derived not typed

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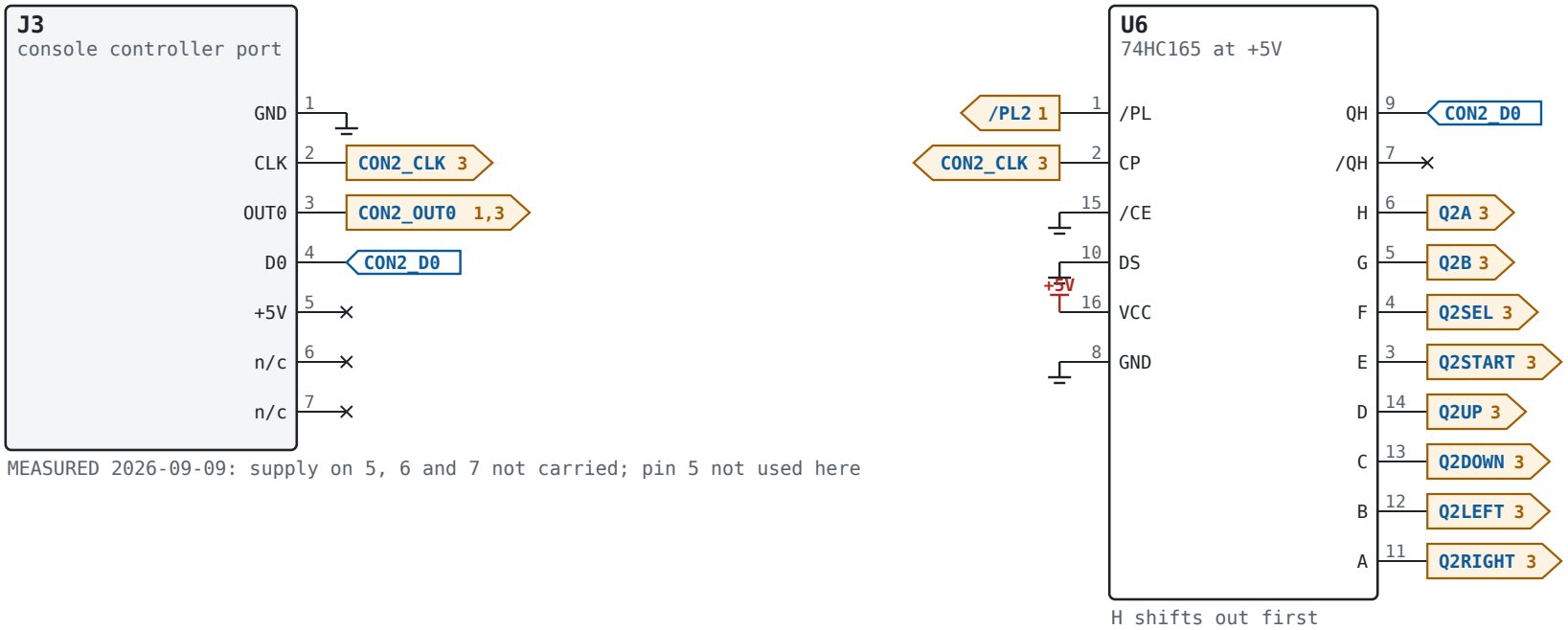
SHEET TITLE
Bridge v2b, sheet 1: port 1

DRAWING NO.	REV	DATE	SHEET
TM-NESB-002	A	2026-11-04	2 of 9

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

v1b plus a second 165/595 pair on the same SPI chain and an LM1881 whose 5 V outputs go straight into the UNO. 2026-09-09. Not built.

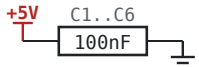
PORT 2: THE SECOND CONSOLE PORT AND ITS REGISTER, ALL AT +5V



MEASURED 2026-09-09: supply on 5, 6 and 7 not carried; pin 5 not used here

H shifts out first

DECOUPLING, AND WHY THE REGISTERS ARE WRITTEN THE WAY THEY ARE



one across each of U1, U2, U5, U6, U7 and U8, at its own supply pins

Two SPI.transfer() calls, port 2's byte first and then port 1's, and one RCLK edge updates both registers together. A tear during a load is impossible, and the firmware still only pulses RCLK while both OUT0 lines read low.
The UNO's outputs are 5 V, so HC parts at 5 V see real highs everywhere. There is not one level shifter on any sheet of this drawing.

bench-v2b-2.svg ansi-a placed at 100% drawn by tools/draw-schematics.py

REV	DATE	REVISION
-	2026-09-08	v2 redrawn for the UNO: no 245, no C6, one rail
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-	2026-09-09	placed and poured as a board, signal traces stil...
A	2026-09-10	four letter sheets, coordinates derived not typed

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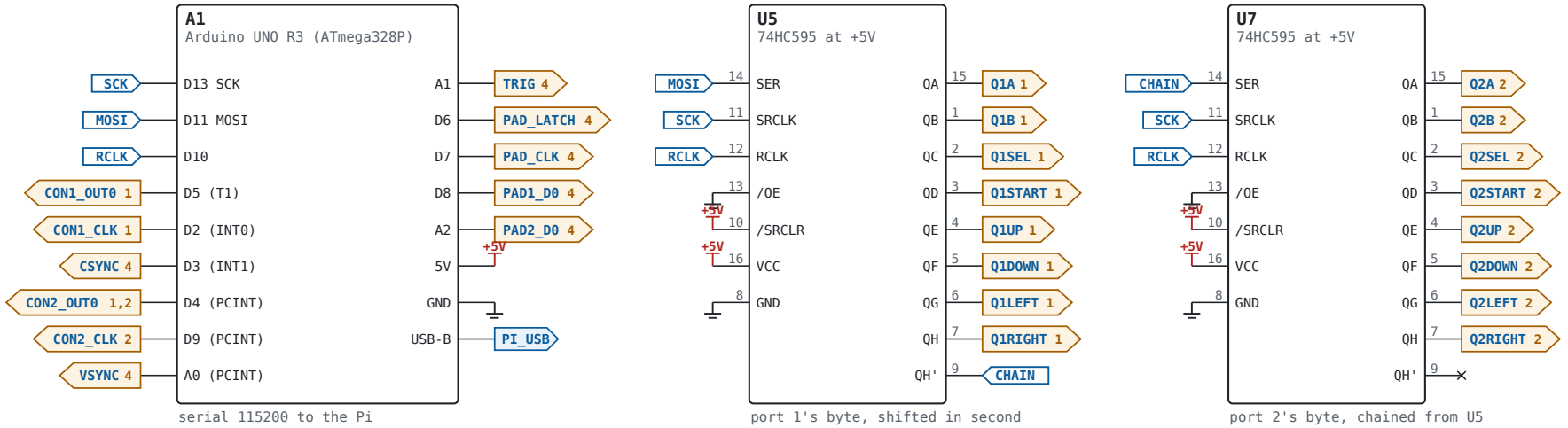
SHEET TITLE
Bridge v2b, sheet 2: port 2

DRAWING NO.	REV	DATE	SHEET
TM-NESB-002	A	2026-11-04	3 of 9

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

v1b plus a second 165/595 pair on the same SPI chain and an LM1881 whose 5 V outputs go straight into the UNO. 2026-09-09. Not built.

THE UNO AND THE TWO OUTPUT REGISTERS ON ONE SPI CHAIN, ALL AT +5V



WHAT COUNTS WHAT, AND THE HEAD

LATCH1 on Timer1's external clock: hardware, and the reference every software count is checked against. CLK1 on INT0, CSYNC on INT1. LATCH2, CLK2 and VSYNC on pin-change ISRs. The 8-per-latch and polls-per-field gates cross-check them; a count that stays green under MUTATE (the D2/D5 jumper swap, D4 the config pin) is a broken count. A1 rises at latch T or at (field, line). L <latch> <byte> <clocks> <t_us> <field> <line>; L2 for port 2; F <field> <t_us> <lines>.

Head and relays, unchanged from v1b. Pi GPIO17 to a PC817 or one TLP281 channel, to the console's reset pads, 100 ms. Pi GPIO27 to the relay module's IN (active low); relay VCC from the Pi's 5 V pin, because the modules on hand are 5 V coil parts. One normally-open contact in series with one lead of the AC adapter cable, never the mains side and never both. Scope: video on CH3, EXT TRIG from R1 (sheet 4), SCPI over the LAN.

bench-v2b-3.svg ansi-a placed at 79% drawn by tools/draw-schematics.py

REV	DATE	REVISION
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A	2026-09-10	four letter sheets, coordinates derived not typed

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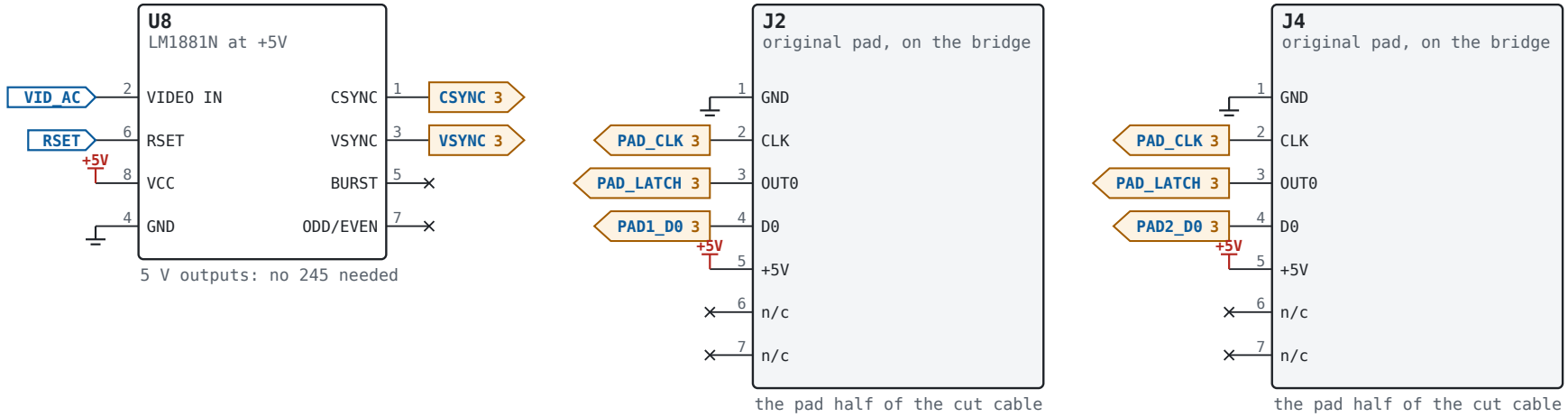
SHEET TITLE
Bridge v2b, sheet 3: the UNO and the registers

DRAWING NO.	REV	DATE	SHEET
TM-NESB-002	A	2026-11-04	4 of 9

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

v1b plus a second 165/595 pair on the same SPI chain and an LM1881 whose 5 V outputs go straight into the UNO. 2026-09-09. Not built.

THE SYNC SEPARATOR, THE BRIDGE'S OWN PADS AND THE TRIGGER, ALL AT +5V



THE PASSIVES ON THIS SHEET



WHERE THESE SIGNALS COME FROM AND WHAT THEY ARE WORTH

C7 AC couples the console's video, tapped after Q1 at the AUX/RF input with a 1k series resistor: the point the scope already probes.
VSYNC: one falling edge per field, 60.0988/s.
CSYNC: one per line plus the vsync block. The NES emits no serrations, so the count per field is lines minus k, and k is measured rather than assumed.

R1 goes to the DS1054Z's rear EXT TRIG. Check the input's rating first; if 5 V exceeds it, a 2:1 divider (two 1k) after R1.
Both pads are polled by the same PAD_LATCH and PAD_CLK and answer on their own D0, so one poll reads both. They are the pad halves of two cut controller cables, and they run at the 5 V they were built for.

bench-v2b-4.svg ansi-a placed at 92% drawn by tools/draw-schematics.py

REV	DATE	REVISION
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A	2026-09-10	four letter sheets, coordinates derived not typed

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SHEET TITLE: **Bridge v2b, sheet 4: sync, the pads and the trigger**

DRAWING NO.	REV	DATE	SHEET
TM-NESB-002	A	2026-11-04	5 of 9

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

Every wire on the board, net by net

Connect everything on a row together. Read back out of the schematic, so it cannot disagree with it.

NET	ENDS	JOIN THESE
+5V	17	U1-14, U2-16, U6-16, C1-1, C2-1, C3-1, C4-1, C5-1, C6-1, A1 5V, U5-10, U5-16, U7-10, U7-16, U8-8, J2-5, J4-5
GND	25	J1-1, U1-7, U2-15, U2-10, U2-8, J3-1, U6-15, U6-10, U6-8, C1-2, C2-2, C3-2, C4-2, C5-2, C6-2, A1 GND, U5-13, U5
/PL1	2	U1-2, U2-1
/PL2	2	U1-4, U6-1
CHAIN	2	U5-9, U7-14
CON1_CLK	3	J1-2, U2-2, A1 D2 (INT0)
CON1_D0	2	J1-4, U2-9
CON1_OUT0	3	J1-3, U1-1, A1 D5 (T1)
CON2_CLK	3	J3-2, U6-2, A1 D9 (PCINT)
CON2_D0	2	J3-4, U6-9
CON2_OUT0	3	U1-3, J3-3, A1 D4 (PCINT)
CSYNC	2	A1 D3 (INT1), U8-1
EXT_TRIG	1	R1-2
MOSI	2	A1 D11 MOSI, U5-14
PAD1_D0	2	A1 D8, J2-4
PAD2_D0	2	A1 A2, J4-4
PAD_CLK	3	A1 D7, J2-2, J4-2
PAD_LATCH	3	A1 D6, J2-3, J4-3
PI_USB	1	A1 USB-B
Q1A	2	U2-6, U5-15
Q1B	2	U2-5, U5-1
Q1DOWN	2	U2-13, U5-5
Q1LEFT	2	U2-12, U5-6
Q1RIGHT	2	U2-11, U5-7

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SHEET TITLE
Wiring list, v2b

DRAWING NO.	REV	DATE	SHEET
TM-NESB-002	A	2026-11-04	6 of 9

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

Every wire on the board, net by net

Connect everything on a row together. Read back out of the schematic, so it cannot disagree with it. Continued from the previous sheet.

NET	ENDS	JOIN THESE
Q1SEL	2	U2-4, U5-2
Q1START	2	U2-3, U5-3
Q1UP	2	U2-14, U5-4
Q2A	2	U6-6, U7-15
Q2B	2	U6-5, U7-1
Q2DOWN	2	U6-13, U7-5
Q2LEFT	2	U6-12, U7-6
Q2RIGHT	2	U6-11, U7-7
Q2SEL	2	U6-4, U7-2
Q2START	2	U6-3, U7-3
Q2UP	2	U6-14, U7-4
RCLK	3	A1 D10, U5-12, U7-12
RSET	3	U8-6, R2-1, C8-1
SCK	3	A1 D13 SCK, U5-11, U7-11
TRIG	2	A1 A1, R1-1
VIDEO	1	C7-1
VID_AC	2	U8-2, C7-2
VSYNC	2	A1 A0 (PCINT), U8-3

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SHEET TITLE
Wiring list, v2b

DRAWING NO.	REV	DATE	SHEET
TM-NESB-002	A	2026-11-04	7 of 9

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

Everything that has to be in a drawer

Parts from every sheet, deduplicated. The status column is the only authored thing in this package's tables.

PART	STATUS	NOTE
74HCT04	on hand	SN74HCT04N, the tube that arrived 2026-09-09
74HC165	on hand	the TI bag. v2b needs a second one
100nF	on hand	v2b runs seven
Arduino UNO R3 (ATmega328P)	on hand	the pile
74HC595	on hand	the box of 30
LM1881N	TO ORDER	the one real order. An old National part, mostly resellers now: buy two
680k	check	LM1881 RSET. One resistor
100R	on hand	the trigger

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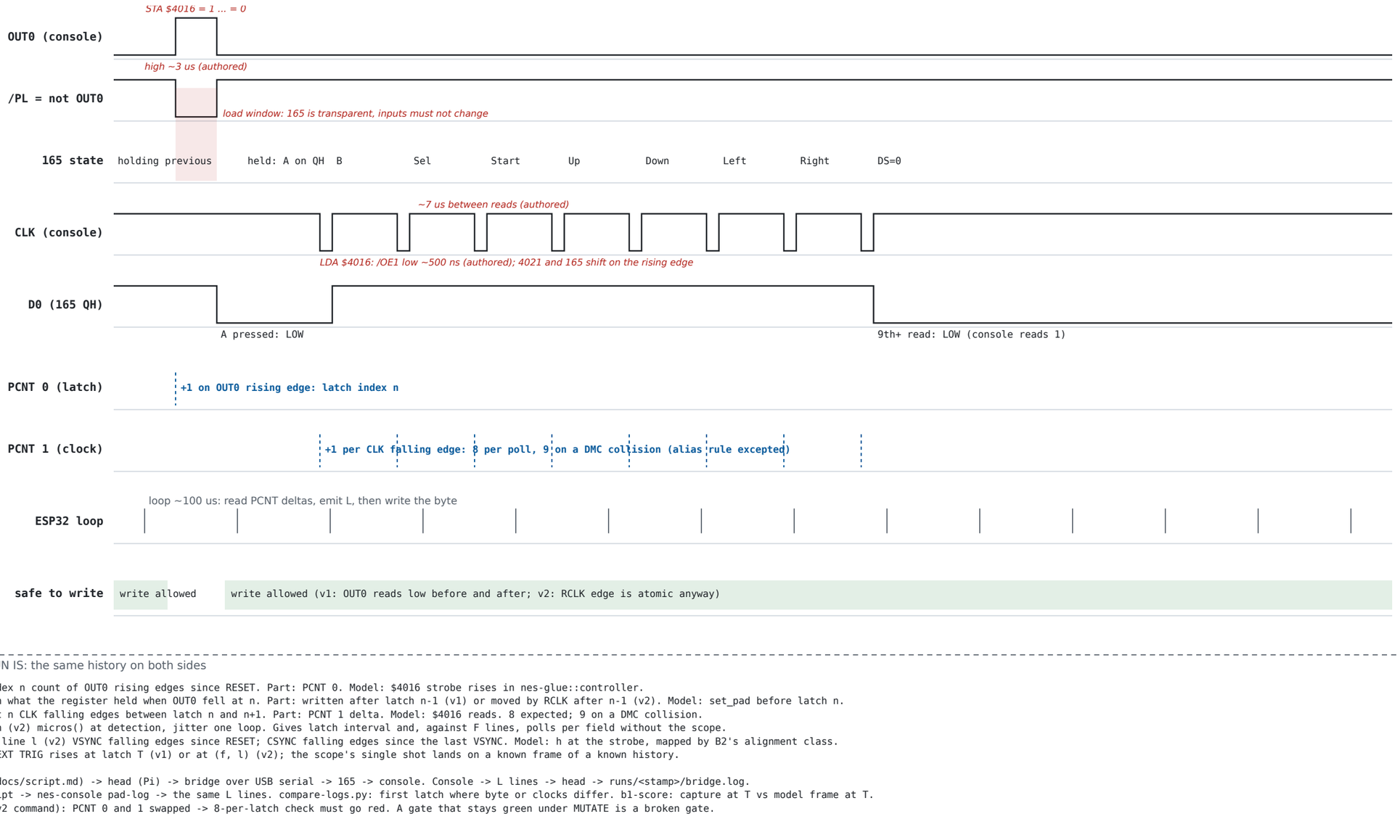
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SHEET TITLE
Parts list

DRAWING NO.	REV	DATE	SHEET
TM-NESB-002	A	2026-11-04	8 of 9

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

timing lanes for one controller read on the part; widths marked authored are B0 measure-first item 3's to replace



WHAT A RUN IS: the same history on both sides

```
latch index n count of OUT0 rising edges since RESET. Part: PCNT 0. Model: $4016 strobe rises in nes-glue::controller.
byte at n what the register held when OUT0 fell at n. Part: written after latch n-1 (v1) or moved by RCLK after n-1 (v2). Model: set_pad before latch n.
clocks at n CLK falling edges between latch n and n+1. Part: PCNT 1 delta. Model: $4016 reads. 8 expected; 9 on a DMC collision.
t_us at n (v2) micros() at detection, jitter one loop. Gives latch interval and, against F lines, polls per field without the scope.
field f, line l (v2) VSYNC falling edges since RESET; CSYNC falling edges since the last VSYNC. Model: h at the strobe, mapped by B2's alignment class.
trigger EXT TRIG rises at latch T (v1) or at (f, l) (v2); the scope's single shot lands on a known frame of a known history.

Script (docs/script.md) -> head (Pi) -> bridge over USB serial -> 165 -> console. Console -> L lines -> head -> runs/<stamp>/bridge.log.
Same script -> nes-console pad-log -> the same L lines. compare-logs.py: first latch where byte or clocks differ. b1-score: capture at T vs model frame at T.
MUTATE (v2 command): PCNT 0 and 1 swapped -> 8-per-latch check must go red. A gate that stays green under MUTATE is a broken gate.
```

logical-timing.svg ansi-b placed at 90% drawn by tools/draw-schematics.py

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SHEET TITLE: **One poll, as timing lanes**

DRAWING NO.	REV	DATE	SHEET
TM-NESB-002	A	2026-11-04	9 of 9

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS