NES controller-port bridge, v1b

The UNO bridge between the Pi and an unmodified NES-001, and the Pi's hands on its reset and power.

Sheets

SHEET	TITLE	PAPER	HOW IT IS MADE
1	Cover and sheet index	letter	this sheet
2	Bridge v1b, sheet 1: the console side	letter	schematic
3	Bridge v1b, sheet 2: the bridge side	letter	schematic
4	Bridge v1b, sheet 3: the head's hands, reset and power	letter	schematic
5	Wiring diagram: every wire at right angles on the packages	ANSI B	schematic
6	Wiring diagram as built: grey is done, a ring needs a check	ANSI B	schematic
7	Wiring diagram, sheet 3: the head's hands at right angles	ANSI B	schematic
8	Breadboard: which hole each part and jumper goes in	ANSI B	schematic
9	Pin map: breakouts, head jumpers, UNO ribbon	letter	schematic, lab log, bring-up tool
10	Pin map: breakouts, head jumpers, UNO ribbon (continued)	letter	schematic, lab log, bring-up tool
11	Wiring list, v1b	letter	derived from the schematic
12	Wiring list, v1b (continued)	letter	derived from the schematic
13	Parts list	letter	derived from the schematic
14	U1, 74HCT04 hex inverter	letter	schematic pins, datasheet purposes
15	U2, 74HC165 shift register, the pad	letter	schematic pins, datasheet purposes
16	U3, 74HC595 output register	letter	schematic pins, datasheet purposes
17	Pin map, sheet 3: the head's jumpers, breakout	letter	schematic, lab log, bring-up tool
18	Pin map, sheet 3: the head's jumpers, breakout (continued)	letter	schematic, lab log, bring-up tool
19	OK1, PC817 module on the reset pads	letter	schematic pins, datasheet purposes
20	K1, relay module in the adapter lead	letter	schematic pins, datasheet purposes
21	Build sequence, sitting 3	letter	derived from the bring-up tool
22	Build sequence, sitting 3 (continued)	letter	derived from the bring-up tool
23	One poll, as timing lanes	ANSI B	schematic

REV	DATE	REVISION
L	2026-09-15	placements drawn: the clock filter and U2's deco...
M	2026-09-15	the register walk reads right through the consol...
N	2026-09-15	sheet 3: the head's hands, reset and power from ...
P	2026-09-23	two index titles shortened: they printed over th...

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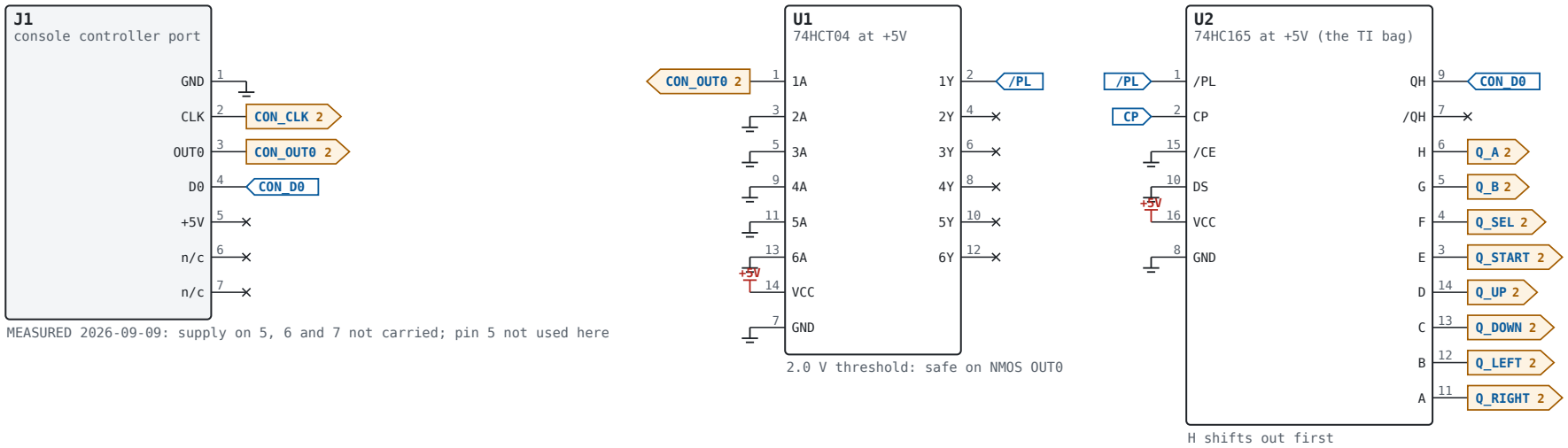
SHEET TITLE
Cover and sheet index

DRAWING NO.	REV	DATE	SHEET
TM-NESB-001	P	2026-11-04	1 of 23

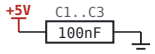
DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

the ATmega328 is a 5 V part, so the register, the pad and the console share one domain. 2026-09-08. Not built; pulse widths authored until B0.

THE CONSOLE PORT, THE INVERTER AND THE REGISTER, ALL AT +5V



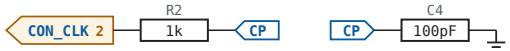
DECOUPLING, AND WHAT THE CONSOLE ACTUALLY DOES



one 100nF across each of U1, U2 and U3, at the chip's own supply pins

OUT0 high: U1 drives /PL low and the 165 loads its eight inputs. It is transparent while low, so the byte must already be in U3 (sheet 2). OUT0 falls, /PL goes high, the byte is held, and QH shows A. Each CLK rising edge shifts the next bit out: B, Select, Start, Up, Down, Left, Right, then DS = GND, so the ninth read and later return 1 as an original pad does. Pressed is LOW, which is what the pad's own 4021 drives.

THE CLOCK PIN, FILTERED (added 2026-09-15)



MEASURED 2026-09-15: a lone pressed bit from B to Left showed on D0 for 50 ns and the register read as if shifted once too often; D0's own falling edge was re-clocking the 165. R2 and C4 (100 ns) sit at pin 2 against a spike that short; the console's clock is microseconds wide and passes. The UNO's D2 still counts CON_CLK ahead of R2.

bench-v1b-1.svg ansi-a placed at 76% drawn by tools/draw-schematics.py

REV	DATE	REVISION
L	2026-09-15	placements drawn: the clock filter and U2's deco...
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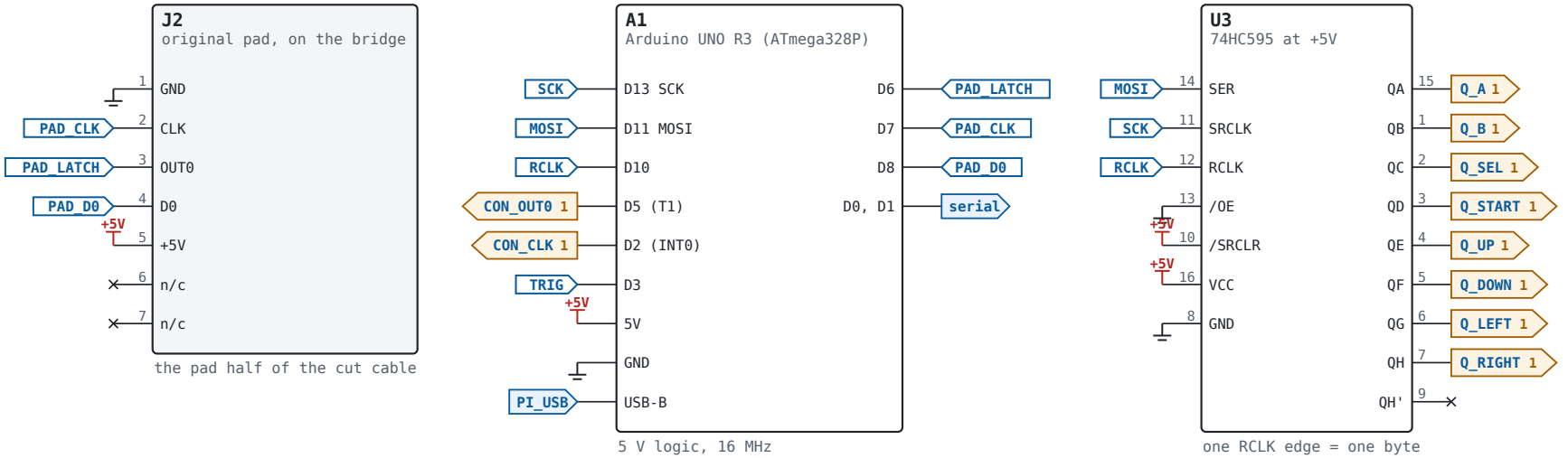
SHEET TITLE
Bridge v1b, sheet 1: the console side

DRAWING NO.	REV	DATE	SHEET
TM-NESB-001	P	2026-11-04	2 of 23

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

the ATmega328 is a 5 V part, so the register, the pad and the console share one domain. 2026-09-08. Not built; pulse widths authored until B0.

THE UNO, THE OUTPUT REGISTER AND THE BRIDGE'S OWN PAD, ALL AT +5V



THE TRIGGER, AND WHY THESE PINS



to the DS1054Z's CH1 (MEASURED 2026-09-15: this scope has no external trigger input; its rear BNC is Trig Out). Trigger on CH1, 2.5 V rising.

D5 is Timer1's external clock input (T1): a 16-bit hardware counter of OUT0 rising edges, which is the latch index. D2 (INT0) takes a falling-edge ISR counting clocks per poll, 480/s, nothing for a 16 MHz part. D3 rises at latch T, one loop late (~100 us); a 74LS74 makes it edge-exact later. SPI clocks 8 bits into U3 in 2 us at 4 MHz and one RCLK edge moves them to its outputs in ~10 ns, so the console never sees half a byte. The firmware still only pulses RCLK while D5 reads low. Serial 115200 to the Pi over USB.

THE HEAD, THE RELAYS AND THE SCOPE (unchanged from v1 except the relay supply)

Pi GPIO17 to a PC817 or one TLP281 channel, to the console's reset pads, 100 ms. Pi GPIO27 to the relay module's IN (active low); relay VCC from the Pi's 5 V pin, because the Songle SRD-05VDC and the Tongling board are 5 V coil parts.

One normally-open contact in series with one lead of the AC adapter cable, never the mains side and never both. Grounds: J1 pin 1, the bridge, the UNO GND and the Pi GND through USB are one net. Scope: video on CH3, the trigger from R1 on CH1, SCPI by LAN.

bench-v1b-2.svg ansi-a placed at 83% drawn by tools/draw-schematics.py

REV	DATE	REVISION
L	2026-09-15	placements drawn: the clock filter and U2's deco...
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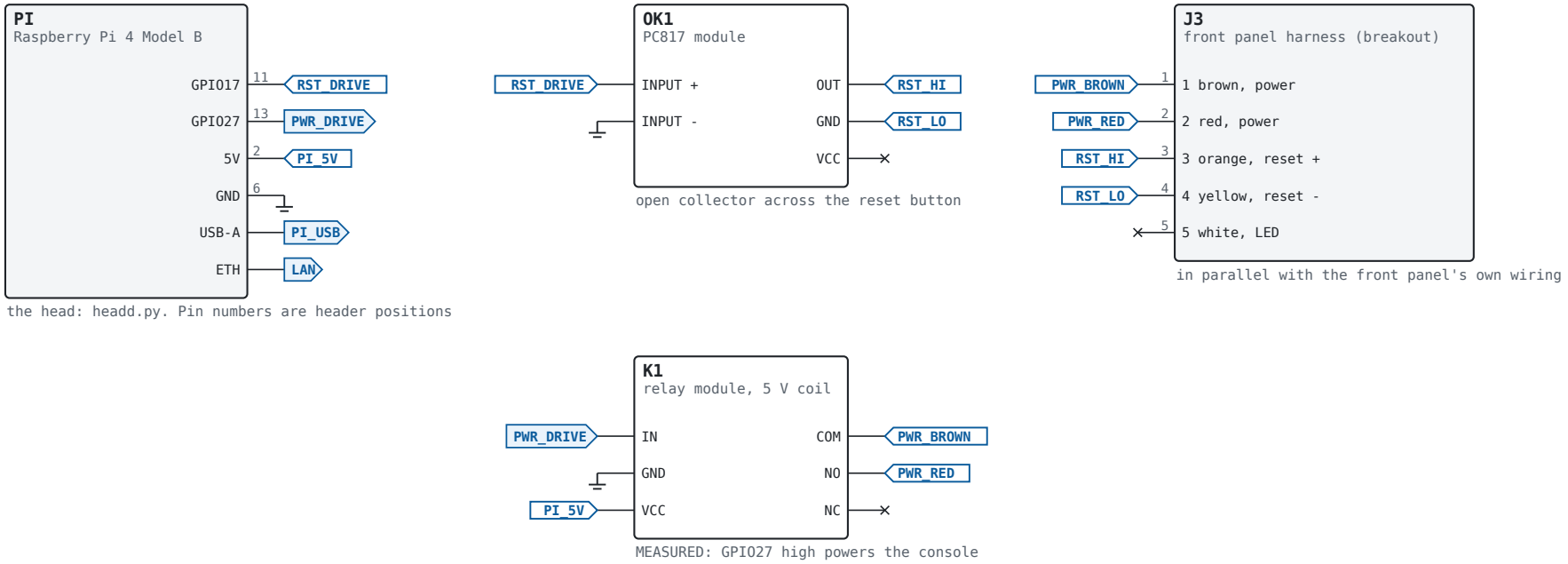
SHEET TITLE
Bridge v1b, sheet 2: the bridge side

DRAWING NO.	REV	DATE	SHEET
TM-NESB-001	P	2026-11-04	3 of 23

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

reset and power from the Pi's header through two modules; the Pi's ground reaches the console through the UNO's USB lead only. Added 2026-09-15.

THE PI'S FOUR JUMPERS, THE OPTOCOUPLER ACROSS THE RESET BUTTON, THE RELAY ACROSS THE POWER SWITCH



WHAT THE HARNESS IS, MEASURED 2026-09-17, AND WHAT IS STILL TO METER

J3 is five ways straight through, colour for colour with the front panel's harness, pin 1 at the back (lab/06-breakout-map-power-reset.jpg), tapped in parallel with the front panel. Metered unpowered by the user: 1 brown and 2 red are the power switch; 3 orange and 4 yellow the reset button; 4 yellow and 5 white the LED. No pin is ground: the front panel is grounded by its pad and the metal housing. OK1's output is a transistor and has a polarity. MEASURED 2026-09-17, console on and the button released: orange sits 4.40 V above yellow, so OUT goes on orange and GND on yellow. Held, the button reads about 200 ohms between them, which a saturated transistor beats. GPIO17 high closes OK1: the reset button, pressed by the head.

K1's contact is in parallel with the front panel's power switch: COM on brown, NO on red (a contact has no polarity). Either closes the console's supply, so the front switch stays OFF while the head runs the power, and does the power by hand while the relay rests open. MEASURED 2026-09-17 at the console, not read off the module: GPIO27 HIGH powers it (video 0.88 Vpp, the port's latch idling at 4.3 V) and LOW turns it off, so the boot config holds GPIO27 LOW and the console rests off. Coil from the Pi's 5 V pin (position 2); GND is 6. The pair carries the adapter's low voltage and the console's current, well inside the contact's 10 A. MAINS SAFETY: nothing on this sheet is ever on the mains side.

bench-v1b-3.svg ansi-a placed at 80% drawn by tools/draw-schematics.py

REV	DATE	REVISION
L	2026-09-15	placements drawn: the clock filter and U2's deco...
M	2026-09-15	the register walk reads right through the consol...
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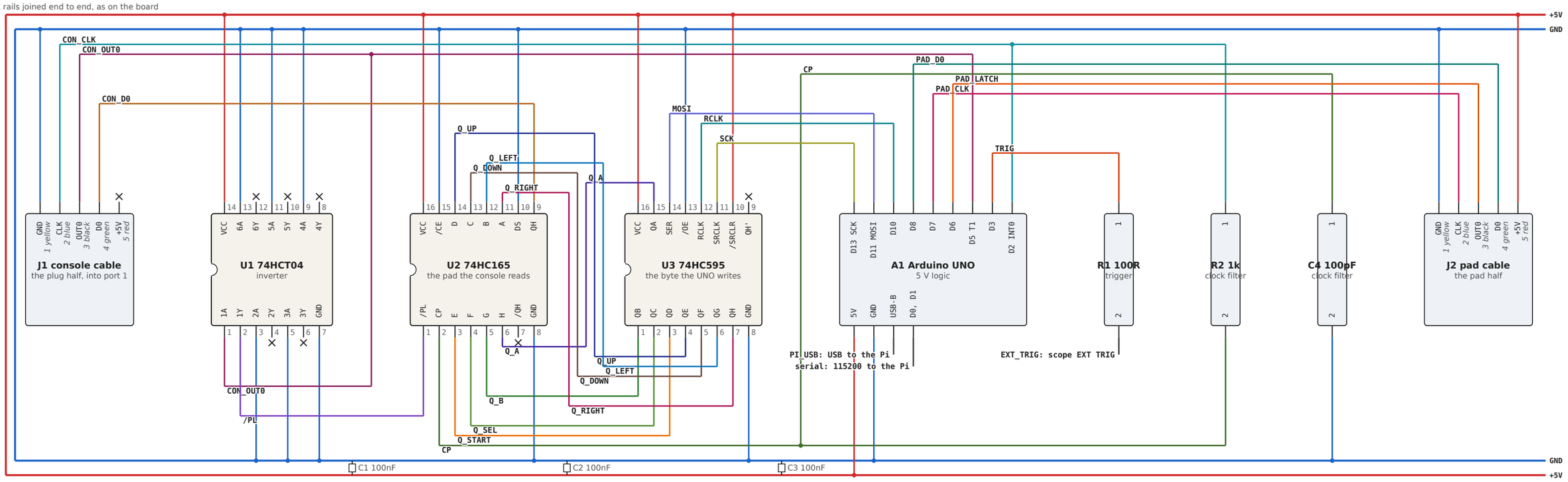
SHEET TITLE
Bridge v1b, sheet 3: the head's hands, reset and power

DRAWING NO.	REV	DATE	SHEET
TM-NESB-001	P	2026-11-04	4 of 23

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

nes-bench — **Wiring diagram: every wire at right angles on the packages**

Notch left, pin 1 bottom left, numbered as the package is. One track and one colour per net, named at its left end; a dot is a junction, a crossing is nothing. Every wire is read out of the schematic.



20 nets on tracks, 7 of them crossing the row; 27 supply pins on the rails. drawn by tools/wiring-diagram.py

wiring-v1b.svg ansi-b placed at 63% drawn by tools/wiring-diagram.py

REV	DATE	REVISION
L	2026-09-15	placements drawn: the clock filter and U2's deco...
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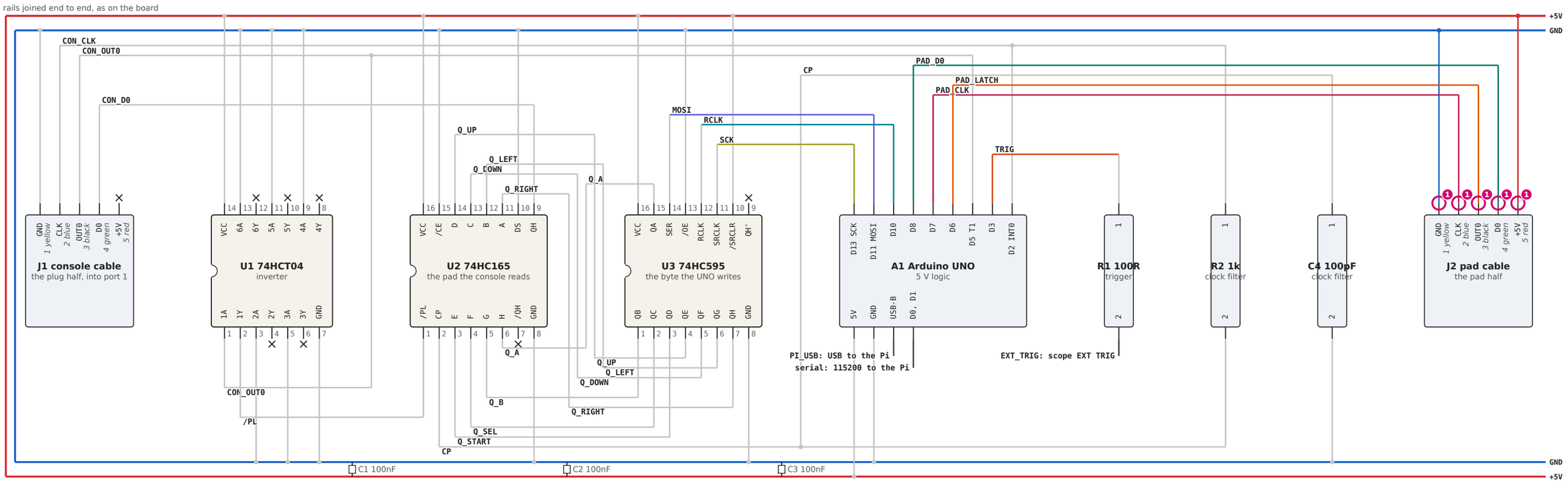
SHEET TITLE: **Wiring diagram: every wire at right angles on the packages**

DRAWING NO.	REV	DATE	SHEET
TM-NESB-001	P	2026-11-04	5 of 23

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

nes-bench — **Wiring diagram as built: grey is done, a ring needs a check**

Grey: built and seen in the right hole. A ring and a number: needs a check, the note under the rails says what. Full colour: not built yet, or not part of this pass.



Needs a check (1)

1. J2, the pad-side housing: LOCATED 2026-09-15 (the pointer): a black housing lying in row j of the middle board's rails side across columns 15 to 10, with the UNO's white, yellow and orange pad leads and the pad cable's five-colour bundle going into it from the frame's right. Which position carries which lead cannot be read from above (the leads enter the housing's

Seen, not on this sheet's nets:

- RIG, SECOND POSE: the boards shifted right on the frame; the map re-read automatically (tools/board-overlay.py --read) and every view re-aimed; the rings sit on the holes out to column 50.
- The middle board is mapped (its rows read the other way up: a to e toward the right board, f to j toward its own rails, the pair below). The five-way housing at columns 9 to 13 is the power and reset breakout's, parked, joined to nothing (the user, 2026-09-15); a 2-by-4 black header stands at the board's left end (columns 58 to 60, rows f to h) and a 4-way header on its rail rows near columns 50 to
- The Q pairing is PROVEN 2026-09-15 23:00: the walk of every single bit through the 595 came back on D0 at its own position, so each grey line joins the 595 output to the 165 input the sheet says.
- The UNO now sits at the frame's top right on a blue screw-terminal shield, its leads running direct: a bundle (purple, blue, cream, red) down over the top rail to U3's rails side and on, a red to the +5V rail at column 5, and white, yellow and orange to the pad's housing on the middle board. The screw shield hides the header's pin labels, so which UNO pin each lead leaves is not readable on camera.
- The two-pin black header across the rail rows at column 27 is a probe point for metering the rail voltage (the user, 2026-09-15): its two pins are not joined to each other, and it is not the UNO's feed.
- Orientation settled: the notch and the pin-1 dot of U1, U2 and U3 all face the high-column end, as the map places them.
- Two yellow ceramic capacitors stand across the rails at columns 28 and 17; the plan puts one 100 nF beside each chip. The value is not readable on camera.
- A red link from the top GND rail row at column 12 runs down to the board's other rail pair: correct but red.

20 nets on tracks, 7 of them crossing the row; 27 supply pins on the rails. drawn by tools/wiring-diagram.py

wiring-v1b-build.svg ansi-b placed at 63% drawn by tools/wiring-diagram.py

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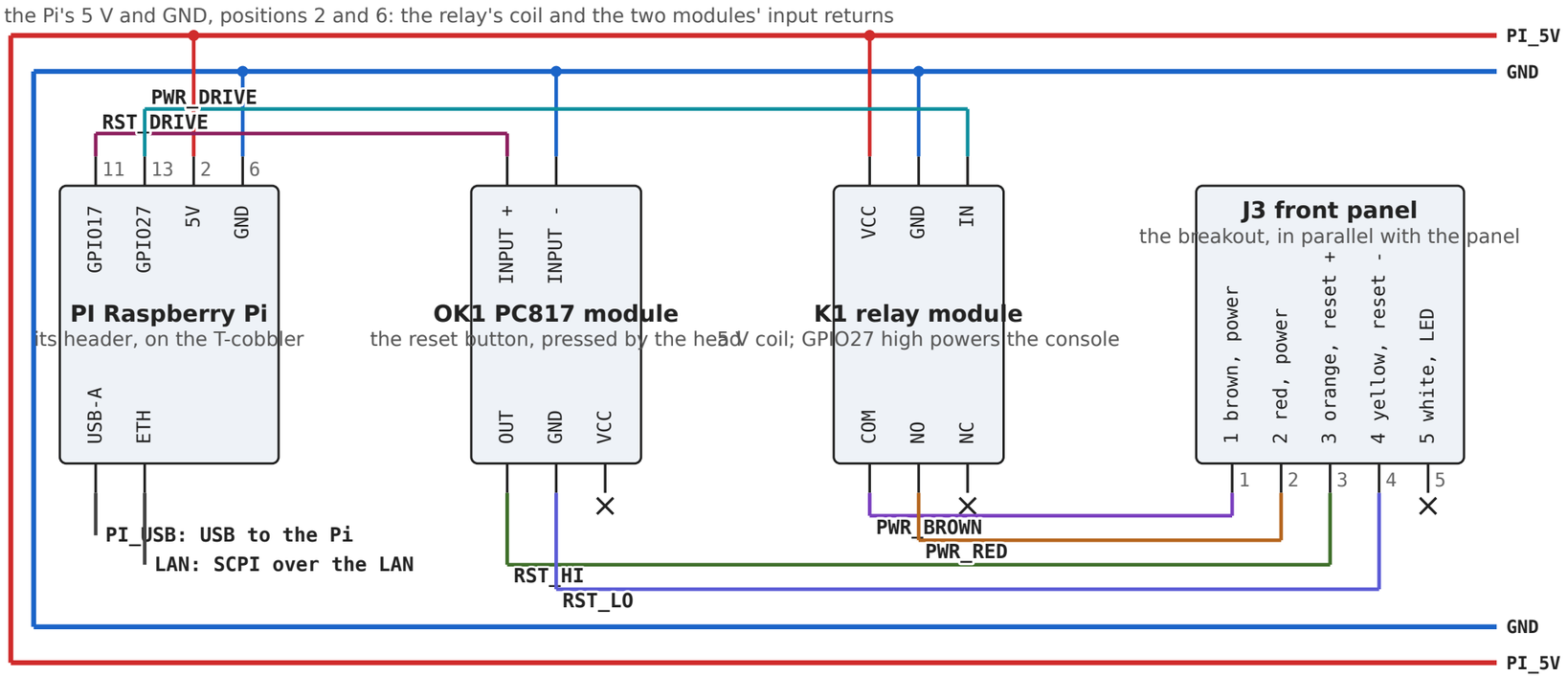
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SHEET TITLE: **Wiring diagram as built: grey is done, a ring needs a check**

DRAWING NO.	REV	DATE	SHEET
TM-NESB-001	P	2026-11-04	6 of 23

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

Sheet 3 of the v1b schematic at right angles. The Pi's pins carry their header positions. Top edges are the Pi's side, bottom edges the console's; the two never meet. Every wire is read out of the schematic.



6 nets on tracks, 0 of them crossing the row; 5 supply pins on the rails. drawn by tools/wiring-diagram.py

wiring-v1b-head.svg ansi-b placed at 108% drawn by tools/wiring-diagram.py

REV	DATE	REVISION
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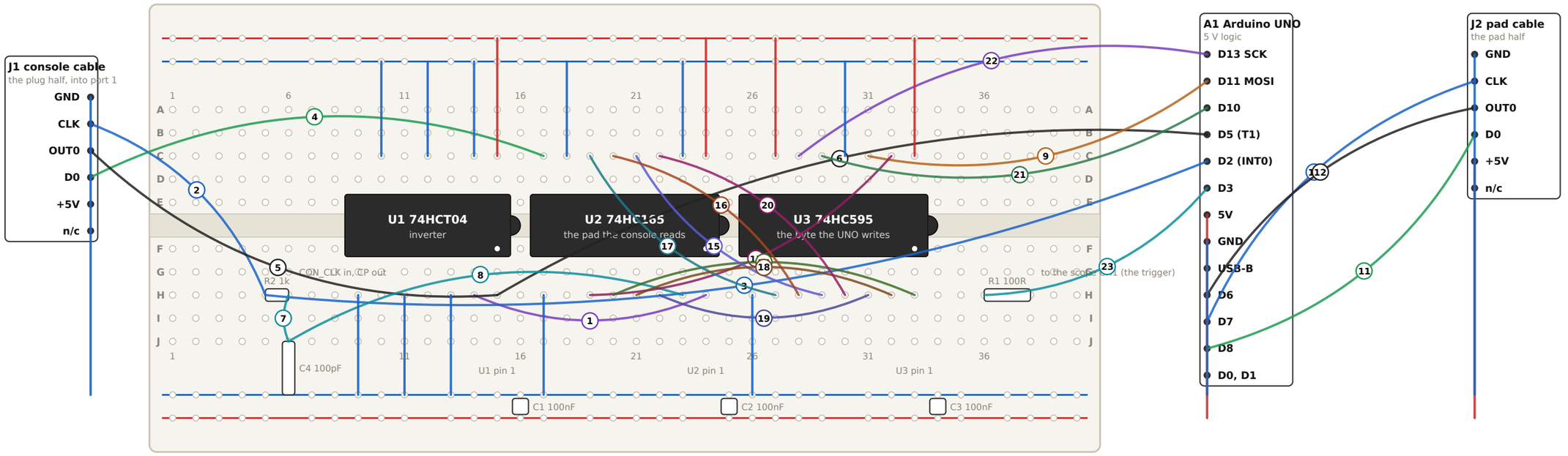
SHEET TITLE: **Wiring diagram, sheet 3: the head's hands at right angles**

DRAWING NO.	REV	DATE	SHEET
TM-NESB-001	P	2026-11-04	7 of 23

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

Bridge v1b on the breadboard: where everything goes

Placement is the board as built on 2026-09-11, read off its photographs: notches toward the high columns, pin 1 lower right. Every wire is read out of the schematic, so this cannot show a connection it does not have.



23 numbered jumpers, and 20 short wires to the rails

Every one of these is read out of the schematic. Red stubs go to the nearest + rail, blue stubs to the nearest - rail; they are not numbered because they are all the same instruction.

1. /PL: U1-2 (col 14 row H) to U2-1 (col 24 row H)
2. CON_CLK, the blue lead: J1 CLK to R2 col 5 row H
3. CON_CLK, the blue lead: R2 col 5 row H to A1 D2 (INT0)
4. CON_D0, the green lead: J1 D0 to U2-9 (col 17 row C)
5. CON_OUT0, the black lead: J1 OUT0 to U1-1 (col 15 row H)
6. CON_OUT0, the black lead: U1-1 (col 15 row H) to A1 D5 (T1)
7. CP: R2 col 6 row H to C4 col 6 row J
8. CP: C4 col 6 row J to U2-2 (col 23 row H)
9. MOSI: U3-14 (col 31 row C) to A1 D11 MOSI
10. PAD_CLK, the blue lead: A1 D7 to J2 CLK
11. PAD_D0, the green lead: A1 D8 to J2 D0
12. PAD_LATCH, the black lead: A1 D6 to J2 OUT0
13. Q_A: U2-6 (col 19 row H) to U3-15 (col 32 row C)
14. Q_B: U2-5 (col 20 row H) to U3-1 (col 33 row H)
15. Q_DOWN: U2-13 (col 21 row C) to U3-5 (col 29 row H)
16. Q_LEFT: U2-12 (col 20 row C) to U3-6 (col 28 row H)
17. Q_RIGHT: U2-11 (col 19 row C) to U3-7 (col 27 row H)
18. Q_SEL: U2-4 (col 21 row H) to U3-2 (col 32 row H)
19. Q_START: U2-3 (col 22 row H) to U3-3 (col 31 row H)
20. Q_UP: U2-14 (col 22 row C) to U3-4 (col 30 row H)
21. RCLK: U3-12 (col 29 row C) to A1 D10
22. SCK: U3-11 (col 28 row C) to A1 D13 SCK
23. TRIG: R1 col 36 row H to A1 D3

breadboard-v1b.svg ansi-b placed at 77% drawn by tools/breadboard.py

REV	DATE	REVISION
L	2026-09-15	placements drawn: the clock filter and U2's deco...
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SHEET TITLE: **Breadboard: which hole each part and jumper goes in**

DRAWING NO.	REV	DATE	SHEET
TM-NESB-001	P	2026-11-04	8 of 23

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

The controller port: pin, NES harness, breakout

Pin numbers are the ones moulded into this console's port housing and the signals are the schematic's, MEASURED 2026-09-09 (the supply is on 5, not 7). Harness colours from the lab log, step 1.1 (2026-09-08). Breakout leads rung out 2026-09-09 with the cable out of the console; the pad half of the cut carries the same five colours. Use the lead, not the colour rule.

PIN	SIGNAL	NES HARNESS	BREAKOUT LEAD	ON THE BRIDGE
1	GND	brown	yellow	the GND rail
2	CLK	red	blue	R2-1, A1 D2 (INT0)
3	OUT0	orange	black	U1-1, A1 D5 (T1)
4	D0	yellow	green	U2-9
5	+5V	white	red	not used: the bridge runs from the UNO's 5 V
6	n/c	blue	not carried	
7	n/c	purple	not carried	

The power and reset breakout

Five ways straight through, colour for colour with the front panel's harness (docs/lab/06-breakout-map-power-reset.jpg), metered 2026-09-17. No way is ground: the front panel is grounded by its pad and housing.

PIN	NES HARNESS	BREAKOUT LEAD	WHAT IT IS
1	brown	brown	power switch
2	red	red	power switch
3	orange	orange	reset, + side (4.40 V)
4	yellow	yellow	reset, - side, and LED
5	white	white	LED

The head's four jumpers

Four Dupont leads off the Pi's header, no breakout (2026-09-10). Header positions are the Pi's own numbering. No wire from here to the console: the Pi's ground reaches it through the UNO's USB cable only.

PI PIN	POS.	TO	ROLE
GPIO17	11	PC817 module INPUT +	reset, 100 ms high
GPIO27	13	relay module IN	power: high is on
5V	2	relay module VCC	the coil's supply
GND	6	PC817 IN-, relay GND	the one ground lent

generated from tools/cheatsheet.py: the schematic, the lab log and tools/bringup.py's lead and ribbon tables

REV	DATE	REVISION
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SHEET TITLE: **Pin map: breakouts, head jumpers, UNO ribbon**

DRAWING NO.	REV	DATE	SHEET
TM-NESB-001	P	2026-11-04	9 of 23

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

The UNO ribbon

Nine Dupont wires from the UNO's digital header, colour per pin as read off the header (2026-09-11). The net and the far end come from the schematic.

UNO PIN	COLOUR	NET	TO
D2	blue	CON_CLK	J1-2, R2-1
D3	green	TRIG	R1-1
D5	yellow	CON_OUT0	J1-3, U1-1
D6	orange	PAD_LATCH	J2-3
D7	red	PAD_CLK	J2-2
D8	brown	PAD_D0	J2-4
D10	black	RCLK	U3-12
D11	white	MOSI	U3-14
D13	grey	SCK	U3-11

generated from tools/cheatsheet.py: the schematic, the lab log and tools/bringup.py's lead and ribbon tables

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SHEET TITLE
Pin map: breakouts, head jumpers, UNO ribbon

DRAWING NO.	REV	DATE	SHEET
TM-NESB-001	P	2026-11-04	10 of 23

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

Every wire on the board, net by net

Connect everything on a row together. Read back out of the schematic, so it cannot disagree with it.

NET	ENDS	JOIN THESE
+5V	9	U1-14, U2-16, C1-1, C2-1, C3-1, J2-5, A1 5V, U3-10, U3-16
GND	18	J1-1, U1-3, U1-5, U1-9, U1-11, U1-13, U1-7, U2-15, U2-10, U2-8, C1-2, C2-2, C3-2, C4-2, J2-1, A1 GND, U3-13, U
/PL	2	U1-2, U2-1
CON_CLK	3	J1-2, R2-1, A1 D2 (INT0)
CON_D0	2	J1-4, U2-9
CON_OUT0	3	J1-3, U1-1, A1 D5 (T1)
CP	3	U2-2, R2-2, C4-1
EXT_TRIG	1	R1-2
MOSI	2	A1 D11 MOSI, U3-14
PAD_CLK	2	J2-2, A1 D7
PAD_D0	2	J2-4, A1 D8
PAD_LATCH	2	J2-3, A1 D6
PI_USB	1	A1 USB-B
Q_A	2	U2-6, U3-15
Q_B	2	U2-5, U3-1
Q_DOWN	2	U2-13, U3-5
Q_LEFT	2	U2-12, U3-6
Q_RIGHT	2	U2-11, U3-7
Q_SEL	2	U2-4, U3-2
Q_START	2	U2-3, U3-3
Q_UP	2	U2-14, U3-4
RCLK	2	A1 D10, U3-12
SCK	2	A1 D13 SCK, U3-11
TRIG	2	A1 D3, R1-1

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tinymachines nes-bench

SHEET TITLE
Wiring list, v1b

DRAWING NO.	REV	DATE	SHEET
TM-NESB-001	P	2026-11-04	11 of 23

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

Every wire on the board, net by net

Connect everything on a row together. Read back out of the schematic, so it cannot disagree with it. Continued from the previous sheet.

NET	ENDS	JOIN THESE
serial	1	A1 D0, D1

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SHEET TITLE
Wiring list, v1b

DRAWING NO.	REV	DATE	SHEET
TM-NESB-001	P	2026-11-04	12 of 23

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

Everything that has to be in a drawer

Parts from every sheet, deduplicated. The status column is the only authored thing in this package's tables.

PART	STATUS	NOTE
74HCT04	on hand	SN74HCT04N, the tube that arrived 2026-09-09
74HC165	on hand	the TI bag. v2b needs a second one
100nF	on hand	v2b runs seven
1k	on hand	R2, the clock pin's series element, placed 2026-09-15
100pF	on hand	C4, the clock pin's filter, placed 2026-09-15
Arduino UNO R3 (ATmega328P)	on hand	the pile
74HC595	on hand	the box of 30
100R	on hand	the trigger

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SHEET TITLE
Parts list

DRAWING NO.	REV	DATE	SHEET
TM-NESB-001	P	2026-11-04	13 of 23

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

U1: 74HCT04 at +5V

Hex inverter, six independent gates. HCT inputs switch at TTL levels (high from 2.0 V), which is why it sits on the console's NMOS OUT0 line: OUT0 high loads the register, so its inversion is the 165's active-low load. One gate is used. The other five inputs are CMOS and must not float: tie each spare A input to GND and leave its Y open.

PIN	NAME	ON THE PART	ON THIS BENCH
1	1A	gate 1 input	CON_OUT0: J1-3, A1 D5 (T1)
2	1Y	gate 1 output, the inverse of 1A	/PL: U2-1
3	2A	gate 2 input	the GND rail
4	2Y	gate 2 output	no connection
5	3A	gate 3 input	the GND rail
6	3Y	gate 3 output	no connection
7	GND	ground	the GND rail
8	4Y	gate 4 output	no connection
9	4A	gate 4 input	the GND rail
10	5Y	gate 5 output	no connection
11	5A	gate 5 input	the GND rail
12	6Y	gate 6 output	no connection
13	6A	gate 6 input	the GND rail
14	VCC	supply, 4.5 to 5.5 V; 100 nF to GND at the pin	the +5V rail

pin purposes authored from the datasheet in tools/cheatsheet.py; the bench column is read out of the schematic

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SHEET TITLE
U1, 74HCT04 hex inverter

DRAWING NO.	REV	DATE	SHEET
TM-NESB-001	P	2026-11-04	14 of 23

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

U2: 74HC165 at +5V (the TI bag)

8-bit parallel-in, serial-out shift register: the pad's 4021 in a 74 package. While /PL is low the eight inputs A to H are copied into the stages as they are (it is transparent, so the byte must be settled before the load). With /PL high, each rising edge of CP shifts one place toward QH and pulls DS in at A. QH shows stage H, so H is the first bit out and A the eighth, which is why the pad's order A, B, Select, Start, Up, Down, Left, Right is wired H down to A. /CE high holds the clock off.

PIN	NAME	ON THE PART	ON THIS BENCH
1	/PL	parallel load, active low: inputs copied in while low	/PL: U1-2
2	CP	shift clock, rising edge, when /CE is low	CP: R2-2, C4-1
3	E	parallel input E, the fourth bit out	Q_START: U3-3
4	F	parallel input F, the third bit out	Q_SEL: U3-2
5	G	parallel input G, the second bit out	Q_B: U3-1
6	H	parallel input H, the first bit out (QH after a load)	Q_A: U3-15
7	/QH	inverted serial output	no connection
8	GND	ground	the GND rail
9	QH	serial output: stage H	CON_D0: J1-4
10	DS	serial in: shifts into A after the eighth clock	the GND rail
11	A	parallel input A, the eighth bit out	Q_RIGHT: U3-7
12	B	parallel input B, the seventh bit out	Q_LEFT: U3-6
13	C	parallel input C, the sixth bit out	Q_DOWN: U3-5
14	D	parallel input D, the fifth bit out	Q_UP: U3-4
15	/CE	clock enable, active low: high inhibits CP	the GND rail
16	VCC	supply, 2 to 6 V; 100 nF to GND at the pin	the +5V rail

pin purposes authored from the datasheet in tools/cheatsheet.py; the bench column is read out of the schematic

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SHEET TITLE
U2, 74HC165 shift register, the pad

DRAWING NO.	REV	DATE	SHEET
TM-NESB-001	P	2026-11-04	15 of 23

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

U3: 74HC595 at +5V

8-bit serial-in, parallel-out shift register with an output latch. Each rising edge of SRCLK shifts SER in at QA's stage; the stages are invisible until a rising edge of RCLK copies all eight into the output latch at once, which is what makes a byte atomic to the console: the 165 never sees a half-written byte. /OE low turns the outputs on; /SRCLR low clears the shift stages (not the latch). QH' is the eighth stage, for chaining a second 595.

PIN	NAME	ON THE PART	ON THIS BENCH
1	QB	latched output B	Q_B: U2-5
2	QC	latched output C	Q_SEL: U2-4
3	QD	latched output D	Q_START: U2-3
4	QE	latched output E	Q_UP: U2-14
5	QF	latched output F	Q_DOWN: U2-13
6	QG	latched output G	Q_LEFT: U2-12
7	QH	latched output H	Q_RIGHT: U2-11
8	GND	ground	the GND rail
9	QH'	stage H unlatched: serial out for a chained 595	no connection
10	/SRCLR	shift register clear, active low: tie high to run	the +5V rail
11	SRCLK	shift clock, rising edge: SER into A, A into B, and on	SCK: A1 D13 SCK
12	RCLK	latch clock, rising edge: all eight stages to the outputs	RCLK: A1 D10
13	/OE	output enable, active low: low drives QA to QH	the GND rail
14	SER	serial data in, sampled on SRCLK's rising edge	MOSI: A1 D11 MOSI
15	QA	latched output A	Q_A: U2-6
16	VCC	supply, 2 to 6 V; 100 nF to GND at the pin	the +5V rail

pin purposes authored from the datasheet in tools/cheatsheet.py; the bench column is read out of the schematic

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SHEET TITLE
U3, 74HC595 output register

DRAWING NO.	REV	DATE	SHEET
TM-NESB-001	P	2026-11-04	16 of 23

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

Every wire on sheet 3

One row per net, read off the schematic. RST_HI is 3 orange and RST_LO is 4 yellow, the reset button, orange the higher of the two. PWR_BROWN and PWR_RED put the relay across the front panel's power switch, which stays off while the head runs the power.

NET	FROM	TO
LAN	PI ETH	SCPI over the LAN
PI_USB	PI USB-A	USB to the Pi
PWR_BROWN	K1 COM	J3-1 1 brown, power
PWR_DRIVE	PI GPIO27 (position 13)	K1 IN
PWR_RED	K1 NO	J3-2 2 red, power
RST_DRIVE	PI GPIO17 (position 11)	OK1 INPUT +
RST_HI	OK1 OUT	J3-3 3 orange, reset +
RST_LO	OK1 GND	J3-4 4 yellow, reset -
GND	PI GND (position 6)	OK1 INPUT -; K1 GND
PI_5V	PI 5V (position 2)	K1 VCC

generated from tools/cheatsheet.py: the schematic, the lab log and tools/bringup.py's lead and ribbon tables

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SHEET TITLE
Pin map, sheet 3: the head's jumpers, breakout

DRAWING NO.	REV	DATE	SHEET
TM-NESB-001	P	2026-11-04	17 of 23

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

The head's four jumpers

Four Dupont leads off the Pi's header, no breakout (2026-09-10). Positions are the Pi's own numbering, odd on the inside row; the far end is read off sheet 3. No wire from here to the console: the Pi's ground reaches it through the UNO's USB cable only.

PI PIN	POS.	TO	ROLE
5V	2	the PI_5V rail	the coil's supply
GND	6	the GND rail	the one ground lent
GPIO17	11	OK1 INPUT +	reset, 100 ms high
GPIO27	13	K1 IN	power: high is on

The power and reset breakout, J3

Five ways straight through, colour for colour with the front panel's harness, pin 1 at the back, tapped in parallel with the panel. What each way is was metered 2026-09-17; no way is ground. Orange sits 4.40 V above yellow with the console on and the button released (2026-09-17), so OK1's OUT goes on orange and its GND on yellow.

PIN	NES HARNESS	BREAKOUT LEAD	WHAT IT IS
1	brown	brown	power switch
2	red	red	power switch
3	orange	orange	reset, + side (4.40 V)
4	yellow	yellow	reset, - side, and LED
5	white	white	LED

generated from tools/cheatsheet.py: the schematic, the lab log and tools/bringup.py's lead and ribbon tables

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SHEET TITLE: **Pin map, sheet 3: the head's jumpers, breakout**

DRAWING NO.	REV	DATE	SHEET
TM-NESB-001	P	2026-11-04	18 of 23

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

OK1: PC817 module

One optocoupler on a carrier: an LED behind a series resistor on the input side, a phototransistor on the output side, nothing joining the two but light. The carrier adds a pull-up from OUT to VCC; with VCC left open OUT is the bare collector and GND the emitter, so the output side is a switch to its own GND and nothing more: the reset button, closed by the head. INPUT + high (3.3 V from a Pi pin is enough) lights the LED and closes the switch.

SIDE	PIN	ON THE PART	ON THIS BENCH
input	INPUT +	LED anode via the series resistor: high turns it on	RST_DRIVE: PI GPIO17 (position 11)
input	INPUT -	LED cathode, the input side's return	the GND rail
output	OUT	collector: pulled to GND while the LED is lit	RST_HI: J3-3
output	GND	emitter, the output side's own ground	RST_LO: J3-4
output	VCC	pull-up supply for OUT; open, so OUT is open collector	no connection: left open on purpose

pin purposes authored from the datasheet in tools/cheatsheet.py; the bench column is read out of the schematic

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SHEET TITLE
OK1, PC817 module on the reset pads

DRAWING NO.	REV	DATE	SHEET
TM-NESB-001	P	2026-11-04	19 of 23

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

K1: relay module, 5 V coil

A 5 V coil relay on a carrier with an opto-isolated input, driving the coil's transistor. The coil takes about 80 mA from VCC, which is why it is on the Pi's 5 V pin and not a GPIO. The contact is a changeover, COM to NO or NC. MEASURED 2026-09-17 at the console rather than read off the module: GPIO27 HIGH powers the console and LOW turns it off, which is why the boot config rests it low.

SIDE	PIN	ON THE PART	ON THIS BENCH
coil	VCC	coil and carrier supply, 5 V	the PI_5V rail
coil	GND	coil and carrier return	the GND rail
coil	IN	control: GPIO27 high is the console on (measured)	PWR_DRIVE: PI GPIO27 (position 13)
contact	COM	the contact's common	PWR_BROWN: J3-1
contact	NO	normally open: meets COM while the coil is on	PWR_RED: J3-2
contact	NC	normally closed: meets COM while the coil is off	no connection: left open on purpose

pin purposes authored from the datasheet in tools/cheatsheet.py; the bench column is read out of the schematic

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SHEET TITLE
K1, relay module in the adapter lead

DRAWING NO.	REV	DATE	SHEET
TM-NESB-001	P	2026-11-04	20 of 23

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

The bridge, built

The breadboard, in two halves that are tested apart before they are joined.

1. 3.1 U1 and U2 on the board, links on H..A, the pattern on QH
2. Console OFF. Build only the console-facing half on the breadboard:
3. The supply is the UNO's own 5 V pin, fed by its USB from the Pi, and NOT the console's pin 7. v1b is one 5 V domain (the schematic's first sheet says so), and the console shares only ground: its pin 1 to the UNO's GND. That is also the only 5 V available, because the breakout does not bring pin 7 out.
4. Leads, from step 1.1's rung-out map: yellow GND, blue CLK, black OUT0, green D0, red +5V. Use the marks on the leads, not the port pin numbers, and not the published pinout.
5. 74HCT04 (U1): pin 14 to the UNO's 5V, pin 7 to GND, pin 1 from the BLACK lead (OUT0).
6. 74HC165 (U2): pin 16 to the UNO's 5V, pin 8 to GND, pin 15 (/CE) to GND, pin 10 (DS) to GND, pin 1 (/PL) from U1 pin 2, pin 2 (CP) from the BLUE lead (CLK), pin 9 (QH) to the GREEN lead (D0).
7. The YELLOW lead is the ground the UNO shares with the console. Nothing goes on the RED lead: it is the console's own 5 V and this bridge runs from the UNO's.
8. 100 nF across each chip's supply pins.
9. Wire links on the eight inputs to make a KNOWN byte. In pad order A, B, Select, Start, Up, Down, Left, Right those are pins 6, 5, 4, 3, 14, 13, 12, 11, and LOW is pressed.
10. Scope CH1 still on OUT0, CH2 moved to QH (U2 pin 9). Console on, game running.
11. 4.1 The UNO drives the 595, measured on its outputs
12. Console OFF and its port half left alone. On the UNO's side of the board:
13. 74HC595 (U3): pin 16 to the UNO's 5V, pin 8 to GND, pin 13 (/OE) to GND, pin 10 (/SRCLR) to 5V, pin 14 (SER) from UNO D11, pin 11 (SRCLK) from UNO D13, pin 12 (RCLK) from UNO D10.

generated from tools/bringup.py, which is also the tool that runs these steps

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SHEET TITLE
Build sequence, sitting 3

DRAWING NO.	REV	DATE	SHEET
TM-NESB-001	P	2026-11-04	21 of 23

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

The bridge, built

The breadboard, in two halves that are tested apart before they are joined. Continued from the previous sheet.

14. 100 nF across its supply pins.

15. Do NOT join U3's outputs to U2's inputs yet. Meter on QA (pin 15), black on GND.

16. 4.2 The original pad polled by the bridge at 5 V

17. This is the PAD HALF of the cut controller cable, the one that does NOT beep to the console's board header, with the pad on the end of it.

18. Its leads carry the same colours as the plug half, because it is the same cable: yellow GND, blue CLK, black OUT0, green D0, red +5V.

19. yellow to GND, RED to the UNO's 5V (the pad's supply comes from the bridge here, and red IS the supply lead on this cable), black (OUT0) to UNO D6, blue (CLK) to UNO D7, green (D0) to UNO D8.

20. Console still off. The bridge drives this half; the console drives the other.

21. You will be asked to hold buttons; the bridge's own poll should follow them.

generated from tools/bringup.py, which is also the tool that runs these steps

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SHEET TITLE
Build sequence, sitting 3

DRAWING NO.	REV	DATE	SHEET
TM-NESB-001	P	2026-11-04	22 of 23

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS

timing lanes for one controller read on the part; widths marked authored are B0 measure-first item 3's to replace



WHAT A RUN IS: the same history on both sides

```
latch index n count of OUT0 rising edges since RESET. Part: PCNT 0. Model: $4016 strobe rises in nes-glue::controller.
byte at n what the register held when OUT0 fell at n. Part: written after latch n-1 (v1) or moved by RCLK after n-1 (v2). Model: set_pad before latch n.
clocks at n CLK falling edges between latch n and n+1. Part: PCNT 1 delta. Model: $4016 reads. 8 expected; 9 on a DMC collision.
t_us at n (v2) micros() at detection, jitter one loop. Gives latch interval and, against F lines, polls per field without the scope.
field f, line l (v2) VSYNC falling edges since RESET; CSYNC falling edges since the last VSYNC. Model: h at the strobe, mapped by B2's alignment class.
trigger EXT TRIG rises at latch T (v1) or at (f, l) (v2); the scope's single shot lands on a known frame of a known history.

Script (docs/script.md) -> head (Pi) -> bridge over USB serial -> 165 -> console. Console -> L lines -> head -> runs/<stamp>/bridge.log.
Same script -> nes-console pad-log -> the same L lines. compare-logs.py: first latch where byte or clocks differ. b1-score: capture at T vs model frame at T.
MUTATE (v2 command): PCNT 0 and 1 swapped -> 8-per-latch check must go red. A gate that stays green under MUTATE is a broken gate.
```

logical-timing.svg ansi-b placed at 90% drawn by tools/draw-schematics.py

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tinymachines — **nes-bench**

SHEET TITLE: **One poll, as timing lanes**

DRAWING NO.	REV	DATE	SHEET
TM-NESB-001	P	2026-11-04	23 of 23

DRAWN BY	SOURCE	SCALE
bisenbek	git 9c81360	NTS